



PTO/SB/08A (07-05)

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Substitute for form 1449/PTO Modified		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	10/726,902
		Confirmation No.:	4177
		Filing Date:	December 3, 2003
		First Named Inventor:	Mitchell Alsup
		Art Unit:	2183
		Examiner Name:	Fennema, Robert E
Sheet	of	Attorney Docket Number:	5500-88700

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code (if known)			
RF		US-5,381,533	1/10/95	Peleg, et al.	
		US-			
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	Check if English Translation is attached
		Country Code-Number-Kind Code (if known)				
RF	A1	GB 2 381 101	4/23/03			<input type="checkbox"/>
RF	A2	EP 0 957 428	11/17/99			<input type="checkbox"/>

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
RF	A3	International Search Report and Written Opinion for PCT/US2004/039269, mailed December 12, 2005, 11 pages.	<input type="checkbox"/>

Examiner Signature	/Robert Fennema/	Date Considered	08/17/2006
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application. ¹Applicant's unique citation designation number (optional).



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Sheet 1 of 2	Attorney Docket Number: 5500-88700

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		Number-Kind Code (if known)			
RF		US-7,003,629	2/21/06	Alsup	
		US-6,449,714	9/10/02	Sinharoy	
		US-6,339,822	1/15/02	Miller	
		US-6,256,727	7/3/01	McDonald	
		US-6,185,675	2/6/01	Kranich, et al.	
		US-6,345,295	2/02	Beardsley, et al.	
		US-5,930,497	7/99	Cherian, et al.	
		US-6,578,128	6/03	Arsenault, et al.	
		US-6,973,543	12/05	Hughes	
		US-6,823,428	11/23/04	Rodriguez, et al.	
		US-6,167,536	12/00	Moann	
		US-6,357,016	3/02	Rodgers, et al.	
		US-2002/0144101	10/02	Wang, et al.	
		US-2003/0023835	1/03	Kalafatis, et al.	
		US-2004/0083352	4/04	Lee	
		US-2004/0193857	9/04	Miller, et al.	
		US-2005/0125632	6/05	Alsup, et al.	
		US-			

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Sheet 2 of 2	Attorney Docket Number: 5500-88700

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
RF	A1	Yuan Chou, et al., "Instruction Path Coprocessors," March 2000, pp. 1-24.	<input type="checkbox"/>
	A2	Friendly, et al., "Putting the Fill Unit to Work: Dynamic Organizations for Trace Cache Microprocessors," Dept. of Electrical Engineering and Computer Sciences, The Univ. of Michigan, December 1998, 9 pages.	<input type="checkbox"/>
	A3	Bryan Black, et al., "Turboscalar: A High Frequency High IPC Microarchitecture," Dept. of Electrical and Computer Engineering, Carnegie Mellon Univ., June 2000, pp. 1-	<input type="checkbox"/>
	A4	Merten, et al., "An Architectural Framework for Run-Time Optimization," June 2001, pp. 1-43.	<input type="checkbox"/>
	A5	Jourdan, et al., "Increasing the Instruction-Level Parallelism through Data-Flow Manipulation," Intel, 11 pages.	<input type="checkbox"/>
	A6	Hinton, G., et al., "A 0.18-MUM CMOS IA-32 Processor with a 4-GHZ Integer Execution Unit," IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, November 2001, pages. 1617-1627.	<input type="checkbox"/>
	A7	Sanjay J. Patel, et al., "replay: A Hardware Framework for Dynamic Optimization," IEEE, Vol. 50, No. 6, June 2001, pp. 590-608.	<input type="checkbox"/>
	A8	Jacobson, et al., "Instruction Pre-Processing in Trace Processors," IEEE Xplore, January 1999, 6 pages.	<input type="checkbox"/>
	A9	Bryan Black, et al., "The Block-Based Trace Cache," IEEE, 1999, pp. 196-207.	<input type="checkbox"/>
	A10	Palmer, et al., "Fido: A Cache That Learns to Fetch," Proceedings of the 17 th International Conference on Very Large Data Bases, Barcelona, September 1991, pp. 255-264.	<input type="checkbox"/>
↓	A11	Chen et al., "Eviction Based Cache Placement for Storage Caches," USENIX 2003 Annual Technical Conference, (13 pages)	<input type="checkbox"/>
			<input type="checkbox"/>
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